Frequency Agile Wideband Phase Lock Loops for RF-FPGAs

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Abstract: *This project develops PLL macros that use novel digital architectures to achieve a user configurable optimum balance between phase noise, frequency resolution, frequency switching time, and power consumption. The PLL macros are implemented in SiGe BiCMOS to take advantage of the good phase noise and power consumption attributes. The digital nature of the implementation facilitates easy porting to more aggressively scaled processes.*

Keywords: Phase Lock Loop; Frequency Lock Loop; Frequency Hopping; Phase Noise; Voltage-Controlled Oscillator.

Introduction

In the IC industry, programmable mixed-signal circuits have shown that this approach can be extended beyond the digital realm [1]. On these types of devices, engineering change orders can be executed very late in the design cycle. In-field updates to add new capabilities can be delivered in software. Boeing's work under the RF-FPGA effort of DARPA's ART program seeks to bring these same advantages to the RF world. For DoD applications, this is very relevant to provide fast reaction time to evolving battlefield threats with digital FPGA-like RF system reconfiguration.

When creating a configurable block, the major challenges are to balance performance with flexibility. Elegance is achieved through simplicity and clarity in the interface design to the block or through abstraction of complex command sequences to simple programming options. The end goal of an RF-FPGA is not to have the most technologically advanced collection of blocks, but to have a coherent system that has a useful programming interface. The key to FPGA-like systems is the abstraction of function to programmability, initially allowing existing functions to be implemented, but also enabling performance that was not anticipated in the original design.
Frequency synthesis is a critical system design element that can often be overlooked. The LNA, mixers, amplifiers, and filters all provide complex design challenges for trade-offs in power, noise, speed, and area. But a poor frequency source easily degrades system performance in spite of excellent innovation in programmability of the other elements. It is noted that most of the design of the other elements typically proceeds with the assumption of a perfect frequency source. To achieve a successful RF-FPGA implementation, a programmable, high-performance, agile frequency synthesis capability is required.

In order to enable this technology Boeing is developing a PLL toolkit that has two Phase Locked Loops (PLLs), one for fast frequency switching and one with fine frequency resolution. This partitioning of PLL functions in into two implementations allows excellent phase noise performance to be achieved at low power consumption while maintaining needed reconfigurability for RF-FGPA platforms. The PLLs can be used in conjunction to cover an operating range of 800MHz to 6.2GHz, provide for 5uS frequency switching speeds with excellent phase noise performance and very low (-90dBc) output spurious frequency content. Accurate Verilog-AMS behavioral models are also part of the tool kit. This enables designers to evaluate various frequency synthesis options while enabling supporting accurate full system simulation.

Target Performance Space

A key component in the design of programmable systems is the definition of a target application space. A narrowed space may allow highly effective architecture optimizations that greatly increase flexibility without compromising performance. This is particularly true in the RF and mixed-signal spaces. One common method for adding programmability is to add switches. However, clever partitioning and definition of granularity into functional blocks minimizes some of the need for high performance switches.

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14. ABSTRACT
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Column1	Borremans [9]	Tasca [10]	TI lmx2541	Willingham [3]	Lanka [6]	Boeing	Boeing2
Architecture	Delta-Sigma	Delta-Sigma	Multi-Modulus	Multi-Modulus	Injection Locking	SPLL	FLPLL
VCO Out Freq (GHz)	5.0-12.0	2.9 - 4.0	3.48 - 4.0	2.4	3.43-4.49	2.0 - 6.2	2.0 - 6.2
RMS Jitter (fs)	560	400	160	?	?	267	267
Spur (dB)	-48	-42	?	-77	-31	-90	-90
PNoise at 20MHz (dBc/H	-145	-139	-154	~ -140	?	-150	-150
Power (mw)	30	4.5	170	41	14	25	25
Area (sq mm)	0.28	0.22	full chip	3.5	0.27	0.2	0.22
Settling Time (Φs)	>50?	>50?	>50?	5	0.003	2	35
	worst				best		

Table 1 Comparison of Target Applications and Metrics

High programmability does not necessarily imply agility. Agile in this sense is the ability to respond quickly to frequency inputs and also the ability to quickly reconfigure to handle other cases. In the RF-FPGA project, reconfiguration is expected to occur in less than 1us.

Frequency synthesis is one area of an RF-FPGA that is mostly stand-alone in the sense that the blocks are isolated and the outputs feed the other components. The application space is then governed by fixed specifications rather than by application specific requirements. To enable a fair comparison, PLLs are selected from four various standards listed in the literature and from a commercial offering. Within Boeing, classified applications have also been considered and targeted. The basic applications are software defined radios (SDRs) (Borremans [9]), newer standards requiring low integrated phase noise (WiMAX, LTE) (Tasca [10]), HomeRF SWAP networking protocol (Willingham [3]), and WiMedia for UWB (Lanka [6]). Note that WiMAX, LTE, and WiMedia examples are research efforts reporting good performance to the date of publication. The PLLatinum TI lmx2541 is also chosen for comparison. Table 1 shows the metrics. A color coding scheme is used to show worst-case in red and best-case in green. Overall, the two proposed Boeing PLLs will provide near best-in-class performance for a wide range of applications.

The issue of phase coherency can be addressed with the tool kit. Phase coherency is essentially the ability change from one frequency to another and then back with the phase being the same as if no switching had ever occurred. By using various combinations of PLLs, phase coherency can be achieved. Future work will explore ways of achieving coherency through various algorithmic techniques in ultra-low spurious fractional-N synthesis.

PLL Tool-Kit Solution

The net result of the Boeing project is to create a tool-kit for implementing various RF-FPGA solutions. The main contents of the tool-kit are a Fine-Frequency (FF) PLL and a Fast-Switching (FS) PLL. In addition, accurate behavioral models will be provided to allow prototyping of the design.

FF-PLL The Fine-Frequency (FF) PLL consists of a fractional-N PLL loop with spur compensation combined with a separate path for adding or subtracting a relatively low frequency input (typically 20-100 MHz). Performing this frequency combining function with negligible phase degradation using traditional mixers and filters would otherwise be extremely difficult if not impractical. A block diagram of the PLL is shown in Figure 1. Digital blocks that can be synthesized are shaded.

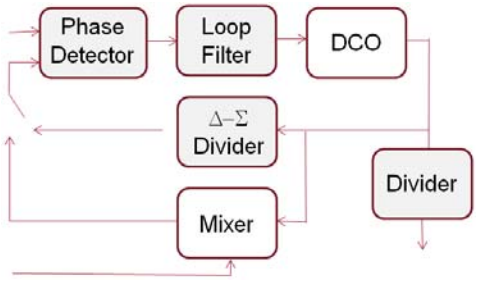

Figure 1 FF PLL Block Diagram

The FF-PLL will have a 10 Hz step size for frequency resolution. This input can be phase-modulated causing the modulation to be imposed on the FF-PLL output. In addition, a low frequency input tone can be summed to cancel the close in phase noise in a dual conversion receiver. Output dividers are provided to support frequency outputs lower than the VCO span.

FS-PLL The Fast-Switching (FS) PLL consists of a phase and frequency locked loop. The frequency locking behavior of the loop provides high frequency (> 1GHz) frequency generation and filtering and high-speed multi-frequency switching capabilities. Applications include creating high-speed low time-jitter clocks for ADCs and DACs, and creation of LOs. A block diagram of the FS-PLL is shown in Figure 2. Again, digital blocks are shaded.

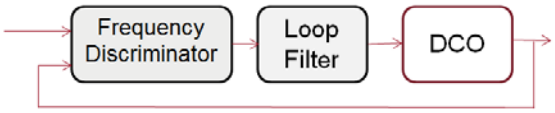

Figure 2 Block Diagram of the FS PLL

Unlike most PLLs, the FS-PLL can filter out a single tone from any number of unwanted tones, effectively creating a narrow, yet agile, phase-domain filter. The loop is a true PLL, combining phase and frequency detection to support true phase locking.

Both PLLs use a common VCO, and basic target specifications are shown in Table 2. The Frequency Switching and Phase Settling times are given for the FS-PLL.

Metric	Stage 1		Stage 2		Units
	Min	Max	Min	Max	
Input Frequency Span	2	4.8	1	6	GHz
Output Frequency Span	2	4.8	1	6	GHz
Frequency Switching Time		25		2	µs
Phase Settling Time		40		5	µs
Residual Phase Noise 1 GHz ≤ f ≤ 3 GHz 3 GHz ≤ f ≤ 6 GHz				 0.20 0.40	°RMS
Output Spurious		-70		–90	dBc
Output Phase Noise Floor		-120		–160	dBc/Hz
Current Consumption		30		25	mA
Closed Loop Bandwidth Reconfigurability	0.1	4	0.1	5	MHz

Table 2 Target PLL Specifications

The flexibility and programmability for the tool-kit is part of the integration process. Two or more PLLs can be combined to create an RF-FPGA synthesis capability. Designers have the flexibility of defining the programming interface in two areas: combined PLL performance and signal routing.

Block-Level Programming Each PLL has individual programmable features governing frequency of operation through input frequency selection or divider value. The VCOs can be digitally calibrated. The FF-PLL can be programmed to be either a frequency summing PLL or a stand-alone fractional-N PLL. PLL bandwidth can be individually set or allowed to be adjusted automatically depending on other programming values. The FS-PLL can be programmed for frequency hopping and for PLL bandwidth.

While the block-level programming interfaces are fixed, the individual blocks can be flexibly defined with standard digital logic (perhaps an FPGA) to provide a custom configuration by the designer. One illustration of designer defined flexibility is in the area of frequency hopping. The interface could be set up in a way that allows a single write or even bit to control frequency hopping and a frequency hopped to. This is a key RF-FPGA toolkit benefit – as components are combined, there is flexibility in adding layers of control to automate some features or make other features have encoding for fast single command execution.

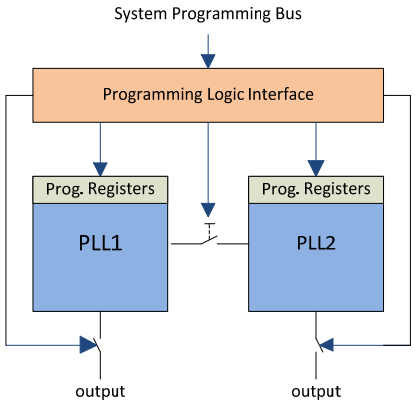

Figure 3 Illustration of a designer created programming interface

A second layer of programmability under designer control is the routing of the output signals from the block. Signals can be gated or routed using switches or muxes. The configuration and programming of this routing is up to the designer, providing maximum flexibility. A case might be where more than two PLLs are included in an RF-FPGA. Output signals might be selected or enabled depending on the current RF-FPGA function. A conceptual example showing both types of configuration are shown in Figure 3.

Behavioral Models System behavioral modeling allows designers to accurately characterize various aspects of a design prior to full implementation. This is achieved by focusing on the important second-order effects when creating the behavioral models.

In the only commercial highly programmable mixed-signal offering [1] [2], it is clear that the people closest to the applications (and not the circuit designers) often have the best insight into what makes a good programmable architecture work. In contrast, it was also true that circuit designers provided some very innovative features that system designers would highly exploit. Architecture evaluation is important and that evaluation needs to be brought into the hands of system designers. System behavioral models are one way of doing this.

Techniques for developing fast and accurate behavioral models are well known [2] [11] [13]. The basic algorithms can be implemented in many languages. Highly accurate models with simulation speed-ups over in SPICE in the 1,000X range are easily possible. Verilog-AMS is chosen in this project. Programmable models are being developed

in the Verilog-AMS language. These models are an essential part of the PLL tool-kit.

Design Portability The current design is being implemented in the IBM 8HP SiGe process. However, most of the PLLs are digital in nature. Digital synthesis is being pursued. Fine line processes such as the 32nm IBM SOI node would allow for higher frequencies and more compact implementation. From an IC and integration point of view, a programmable and portable solution is highly attractive. It is becoming clearer that in aggressively scaled processes, the use of heavily digital, digitally assisted analog solutions is an effective solution for RF-FPGA architectures.

Design Space Illustration

The value of a programmable solution can be judged with several metrics. Perhaps the most powerful is hindsight when a totally unanticipated solution is made possible through software configuration of the underlying hardware. For the RF-FPGA project, a more realistic metric is the breadth of space covered by a solution. When visualizing this space, it becomes possible to realize which existing solutions could be covered and to dream of new solutions.

The behavioral models were combined to begin looking at a space of phase noise vs. frequency of operation vs. lock time. The inverse of lock time is an indicator of frequency hopping speed. A plot of one such visualization is shown in Figure 4.

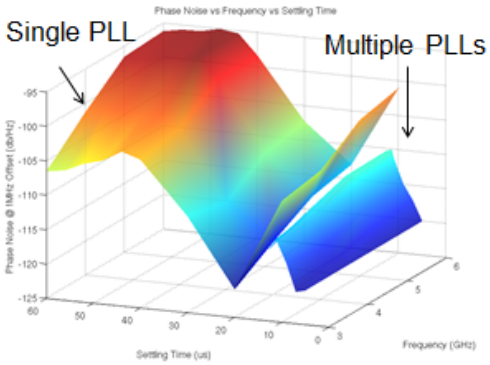

Figure 4 Trade space for Phase Noise, Frequency Output, and Settling Time

Conclusion

This DARPA RF-FPGA effort is currently in it's first year. The Boeing project is working on a yearly timeline of producing Stage 1 and Stage 2 results in August of 2013 and August of 2014. The PLL tool-kit approach provides an extremely portable, agile, and flexible approach that supports state-of-the-art performance for phase noise, power, frequency resolution, and switching time combined with the ability for system designers to innovate and rapidly access system performance to decouple chip design from system implementation of RF systems.

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